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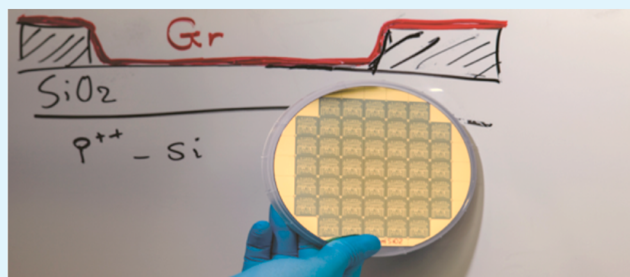
Up-Scaling Graphene Electronics by Reproducible Metal–Graphene Contacts

Kamal Asadi,*[†] Eugene C. Timmering,[‡] Tom C. T. Geuns,[‡] Amaia Pesquera,[§] Alba Centeno,[§] Amaia Zurutuza,[§] Johan H. Klootwijk,[‡] Paul W. M. Blom,[†] and Dago M. de Leeuw[†,‖]

[†]Max-Planck Institute for Polymer Research, Ackermannweg 10, D-55128 Mainz, Germany
[‡]Philips Research Laboratories, High Tech Campus 4, 5656 AE Eindhoven, The Netherlands
[§]Graphenea S.A., Tolosa Hiribidea 76, 20018 Donostia-San Sebastian, Spain
[‖]King Abdulaziz University, Abdullah Sulayman, 22254 Jeddah, Saudi Arabia

Supporting Information



ABSTRACT: Chemical vapor deposition (CVD) of graphene on top of metallic foils is a technologically viable method of graphene production. Fabrication of microelectronic devices with CVD grown graphene is commonly done by using photolithography and deposition of metal contacts on top of the transferred graphene layer. This processing is potentially invasive for graphene, yields large spread in device parameters, and can inhibit up-scaling. Here we demonstrate an alternative process technology in which both lithography and contact deposition on top of graphene are prevented. First a prepatterned substrate is fabricated that contains all the device layouts, electrodes and interconnects. Then CVD graphene is transferred on top. Processing parameters are adjusted to yield a graphene layer that adopts the topography of the prepatterned substrate. The metal–graphene contact shows low contact resistances below 1 kΩ μm for CVD graphene devices. The conformal transfer technique is scaled-up to 150 mm wafers with statistically similar devices and with a device yield close to unity.

KEYWORDS: *graphene transistor, contact resistance, conformal transfer, CTLM, reproducible contact*

INTRODUCTION

Graphene transistors hold great promise for microelectronic applications.[1−10] There is a manifold of challenges, as pointed out by the International Technology Roadmap for Semiconductors, toward integration and up-scaling of graphene electronic devices. One challenge, according to the roadmap, is to develop a CMOS compatible process that enables reproducible formation of low resistance contact.[11]

Like any electronic device Ohmic contacts to graphene with low contact resistances, R_c's, are required for injection and extraction of majority charge carriers.[12] Variation in the contact resistance would lead to parameter spread of the discrete graphene transistors which limits up-scaling and integration.[13] Therefore, a technology is needed that allows formation of reproducible low resistance Ohmic metal–graphene contacts on a wafer-scale, and that yields statistically similar devices with narrow parameter spread.[11]

The contact resistance is usually evaluated with a combination of two and four point probes or by transfer length methods (TLM). The lowest reported contact resistance is 110 ± 20 Ωμm for Pd on exfoliated graphene.[14] Mechanical exfoliation, however, is an inappropriate graphene production technique for industrial up-scaling. Catalytic chemical vapor deposition (CVD), whereby a precursor is decomposed at elevated temperatures of around 1000 °C on large Cu substrates, is an industrially viable graphene production technique.[15] CVD grown graphene can then be transferred to any other substrate after wet etching of the copper.[16] Subsequently, devices are fabricated by conventional top-down processes, i.e., optical photolithography using a UV-light source and deposition of the contact. In Figure 1a, we have provided an overview of the reported contact and sheet resistances of the graphene transistors fabricated with CVD graphene grown on copper or nickel. The metal used for the contact is usually Ti/Au. We note that we have limited the literature review to only transferred CVD graphene. Mechanically exfoliated graphene devices and those based on graphene grown on SiC are excluded for the sake of fair comparison. It is apparent from Figure 1a that there is large scattering in the reported values for R_c and R_{sh}.

It is well-documented in the literature that the conventional device fabrication process steps are invasive and alter the electrical properties of the CVD-graphene layer.[16−28] Direct deposition of metal contacts onto graphene results in damaging

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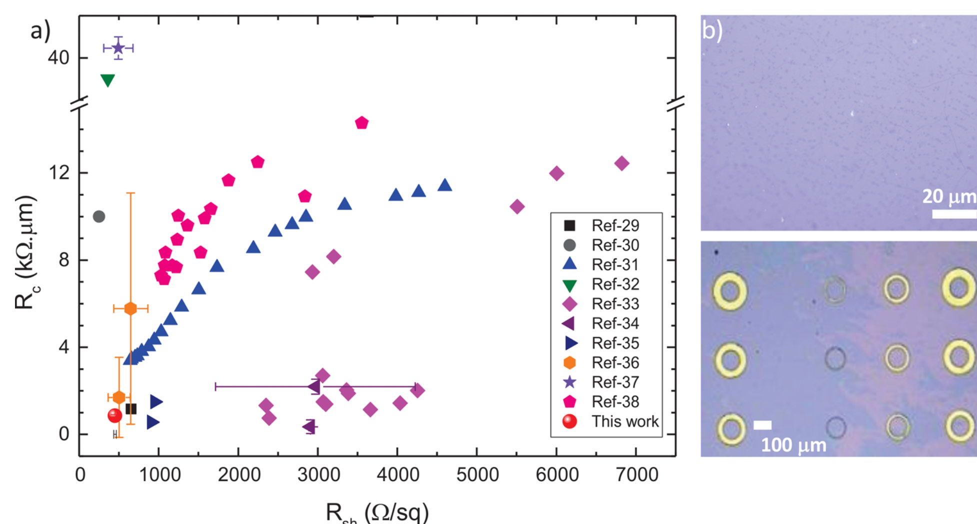

Figure 1. (a) Overview of the reported R_c values as a function of R_{sh} for devices based on CVD grown graphene transferred onto silicon wafer with thermally grown SiO_2 oxide layer. CVD graphene obtained from SiC is excluded. For fair comparison, the device parameters before any post-fabrication-treatments of the contacts are compared. Several contact metals have been examined: ref 29, Cu/graphene; ref 30, Au/Ti/graphene; ref 31, Au/graphene; ref 32, Au/Ti/graphene; ref 33, Au/Pd/Ti/graphene, Au/Ni/graphene, and Au/Ti/graphene; ref 34, Au/Pd/Ti/graphene; ref 35, Al/Cr/Au/graphene; ref 36, Au/Ti/graphene; ref 37, Au/Ti/graphene; ref 38, Au/Ni/graphene. For comparison our data is included in the graph, where both low R_c and R_{sh} have been obtained. (b) In top panel, a photograph of a transferred CVD graphene layer on top of a thermally oxidized silicon wafer is presented. Bottom panel shows the same graphene layer after going through the conventional device fabrication process, i.e., lithography, contact deposition, and then lift-off. The processing resulted in partial removal of the graphene layer as seen by the color contrast on the image. Appearance of processing related defects that lower the device yield significantly is due to low adherence of the graphene layer to the substrate.

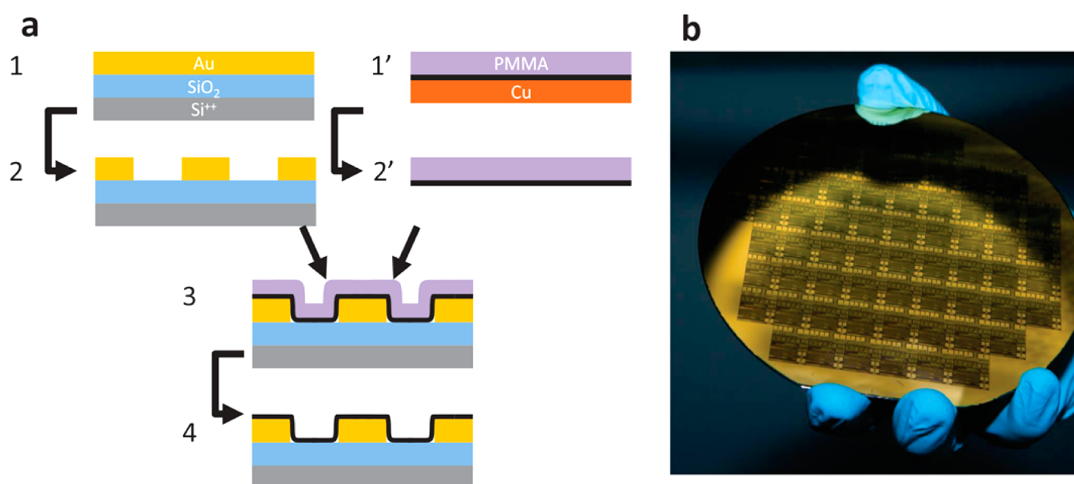

Figure 2. Graphene device fabrication by conformal transfer. (a) At stages 1 and 2 electrodes are defined by conventional photolithography on the wafer. At stages 1′ and 2′, CVD graphene grown on Cu is transferred onto a PMMA carrier layer. Graphene is indicated by the black line. At stage 3, by tuning the transfer parameters, conformal transfer of graphene onto the prepatterned wafer is obtained; finally at stage 4, PMMA is washed away, and the graphene device is obtained. (b) Photograph of a patterned 150 mm wafer with graphene transferred onto the whole area. Patterned Au contacts have a thickness of 150 nm.

and uncontrolled doping of the graphene under the contact area. To show the invasive nature of the conventional processing, in Figure 1b, we present images of a transferred CVD graphene layer on a silicon substrate. Before conventional device processing, it is observed that the graphene layer uniformly covers the substrate. Subsequently, conventional photolithography and gold deposition were performed. After lift-off and realization of patterned gold rings, we have observed that, for a “clean” transferred graphene, due to the weak adhesion of graphene to the substrate, shear forces during the resist coating and lift-off processes remove parts of the transferred graphene layer, as shown in Figure 1b. As a result, up-scaling and reproducing statistically similar devices with CVD graphene is hampered.

To prevent any damage to the graphene by processing, here we introduce conformal graphene transfer, as schematically depicted in Figure 2. First source and drain electrodes and interconnects are processed on a heavily doped 150 mm Si single crystal substrate that serves as the common gate electrode with 250 nm thermally grown oxide. The electrodes are made by standard semiconductor processing: metal deposition and photolithography. Then, a CVD grown graphene monolayer is transferred on top of the prefabricated substrate. With adjustments to the processing parameters, a

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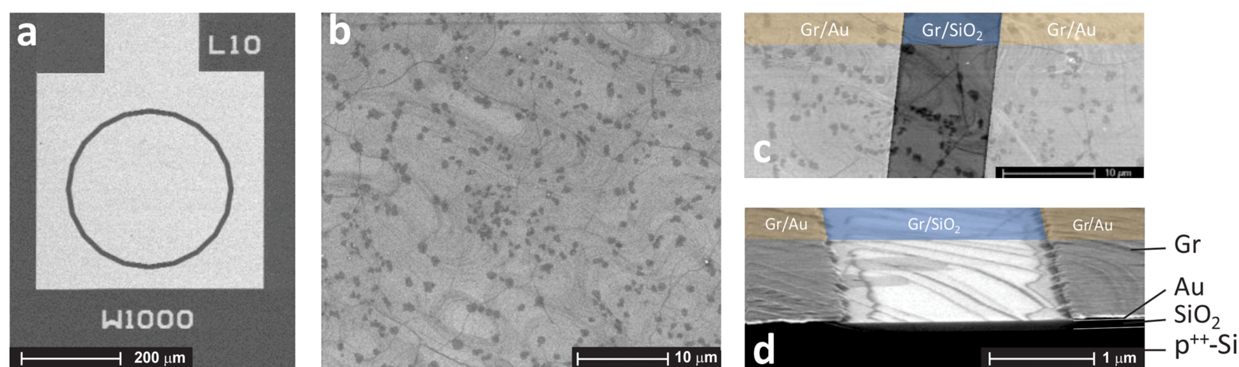

Figure 3. Conformal graphene transfer. (a) A CTLM device with contact spacing and width of 10 and 1000 μm, respectively. (b) SEM picture of the graphene film transferred onto a smooth 150 mm Si monitor wafer. (c) SEM top image of graphene transferred onto a prepatterned substrate. The image shows the Au contacts of the CTLM structure, as well as the area in between the contacts that are uniformly covered with graphene. Different areas are marked, wherein Gr stands for graphene. The channel length is 10 μm. (d) SEM cross-section of the CTLM contact showing the conformal coverage of the graphene.

conformal transfer of graphene was obtained, meaning that the graphene layer adopts the topography of the prepatterned substrate. Direct metal deposition onto graphene is prevented, and processing related structural damage to the CVD graphene layer is minimized. The formation of the contact between metal and graphene is noninvasive. The metal−graphene contacts were investigated using the circular transmission line method (CTLM), which advantageously alleviates the need for patterning of graphene.[39] We show that conformal graphene transfer is a reliable and reproducible fabrication technique for CVD graphene devices. The technique is scaled-up to 150 mm wafers with statistically similar devices and with a device yield of unity.

■ CONFORMAL GRAPHENE TRANSFER

CTLM test structures were fabricated on 150 mm Si wafers with 250 nm of thermally grown SiO_2. The highly doped *p*-type substrate acts as a common gate. Au electrodes of 150 nm thick were defined by conventional I-line photolithography. A 2 nm Ti was used as an adhesion layer. Ti and Au were both deposited by sputtering. The diameter of the inner electrode was kept constant at 319 μm to result in an electrode width of 1000 μm, as shown in Figure 3a, and the electrode spacing systematically varied from 0.75 to 40 μm. The SiO_2 surface was passivated with hexamethyldisilazane (HMDS) prior to conformal graphene transfer.

Graphene was grown on 25 μm Cu foils in a cold walled CVD reactor using methane as precursor. The foils were annealed in a H_2/Ar atmosphere at 1000 °C. Graphene was grown at 1000 °C using a low methane flow and low pressure. Once the growth was complete the graphene was transferred via a wet transfer process by spin-coating a sacrificial poly(methyl methacrylate) (PMMA) layer on the Cu foil. The thickness of the PMMA layer was typically a few micrometers. We note that there can be an inhomogeneity in PMMA layer thickness amounting to maximum 10% of the total thickness. Then, the Cu was etched with a 1 M ferric chloride solution for several hours. After etching, the PMMA/graphene was thoroughly washed twice in fresh deionized water bath. For the transfer to the target substrate, the PMMA/graphene films were floated off in fresh deionized water bath with a submerged substrate. The PMMA/graphene films were very slowly picked up from beneath with unpatterned smooth Si monitor wafer or a prepatterned substrate. After the residual water has evaporated, the PMMA layer was removed with a fresh acetone bath. Subsequently the exposed transferred graphene was washed in a deionized water bath. The final cleaning processes were repeated several times to minimize the PMMA debris. Raman spectra of the transferred graphene are given in the Supporting Information, Figure S1. The spectra show the typical fingerprint of CVD monolayer graphene with only a very small defect peak. Optical microscopy showed almost no transfer debris, Supporting Information Figures S2 and S3. The morphology of transferred graphene onto the monitor wafer was further investigated by scanning electron microscopy (SEM), shown in Figure 3b. The graphene layer is a fully closed monolayer and shows intrinsic features like ridges and islands of second graphene layers, which are inherent to CVD grown graphene.

Subsequently, the transferred graphene onto a prepatterned substrate with an uneven topography was studied by SEM. At the contact edges cracks and therefore a discontinuous layer might be expected. Hence we investigated the morphology and continuity of the graphene layer transferred onto a prepatterned substrate, and compared it with the graphene transferred onto a smooth monitor wafer. The image of Figure 3c shows that the morphology on the Au contact and that on the SiO_2 layer are identical to that of a graphene layer transferred to the monitor wafer, Figure 3b. Extensive inspection of the samples shows that the transfer of the graphene onto a prepatterned wafer with topographical differences does not lead to an increase in extrinsic defects like cracks or film discontinuities. Finally, the SEM cross section of Figure 3d shows that the coverage of graphene is conformal; the transferred graphene follows the topography of the patterned substrate. Because the contacts are square the step coverage is not unity. Figure 2d shows that the area close to the contact that is not covered is comparable to the contact height, yielding a bending angle of the graphene monolayer of about 45°. This means that for long channel lengths the graphene is in close contact with the substrate surface. For a very short channel length suspended graphene with an air gap is expected.

■ CONTACT RESISTANCE

Contact resistances were extracted by CTLM measurements. CTLM, like the conventional TLM technique, also allows extraction of the graphene sheet resistance, R_{sh}, contact

resistance, R_c, and transfer length, L_t. We used CTLM test structure, because it circumvents the need for patterning of graphene.[39−41] We note that CTLM also eliminates parasitic effects such as nonuniform or undefined electric field at the sharp corners.[39] A full description of the TLM and CTLM methods is given in the Supporting Information.

Four point probe measurements were carried out by forcing a constant dc current and measuring the voltage drops across the contacts. Four different current levels, ranging from 10 μA to 10 mA, were applied. Both current injection into the graphene layer and current extraction from the graphene layer were measured. Identical injection and extraction parameters unambiguously show the absence of an injection barrier and, hence, confirm the Ohmicity of the contacts for both forward and reverse bias. Total resistance between the inner and surrounding contact was calculated by dividing the measured voltage drop by the forced current, corrected with a geometrical factor for each device (see Supporting Information).

A typical CTLM resistance plot is given in Figure 4a,b for both current injection/extraction at 1 mA. The resistance

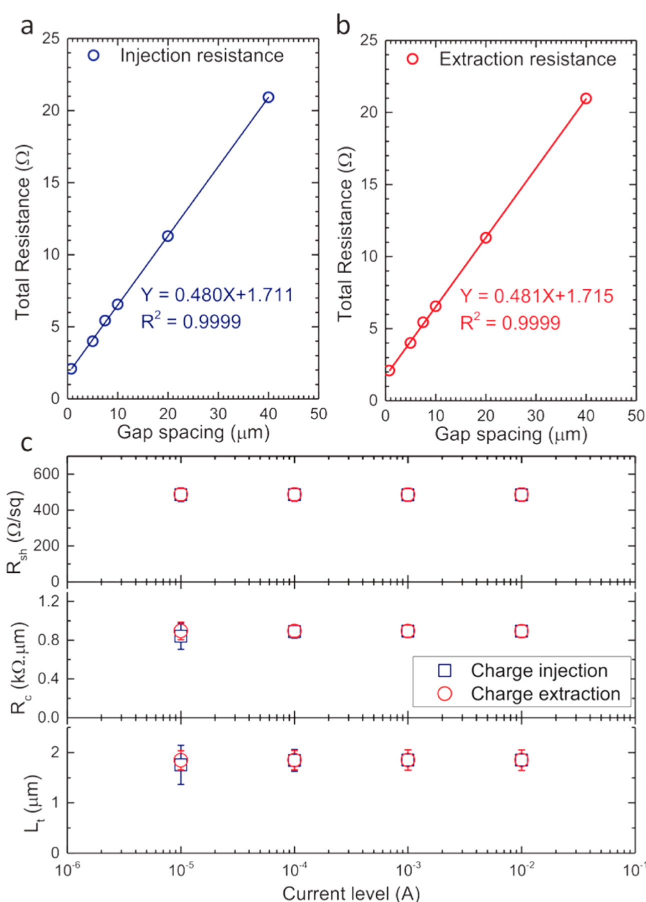

Figure 4. Circular transmission line measurements (CTLM). The resistance between the inner and surrounding contacts as a function of gap spacing between the two electrodes for (a) current injection and (b) current extraction. The gap spacing was varied between 0.75 and 40 μm. The diameter of the inner contact was 319 μm yielding a contact width, W, of 1000 μm. The equations give the linear fit to data with the slope being R_{sh}/W and intercept being $2R_c$. (c) Extracted values for the sheet resistance, R_{sh}, contact resistance, R_c, and transfer length, L_t, as a function of current calculated from CTLM measurements of several test structures, both for charge injection and charge extraction.

increases with electrode spacing. Contact and sheet resistances were determined by least-squares linear fits. Excellent fits are obtained for both current injection and extraction, with R^2 of 0.9999. From the slope of the linear fit, R_{sh} = 480 Ω/□ was obtained, whereas from the intercepts with the resistance and gap spacing axes, R_C = 855 Ω μm and L_t = 1.78 μm for both injection and extraction were obtained. Reported values of R_{sh} for CVD graphene are highly scattered, as shown in Figure 1a, ranging from several hundred Ω/□ to typically a few kΩ/□. Achieving low values for both R_{sh} and R_c indicates that device fabrication by conformal transfer procedure can yield high quality graphene devices with low resistance contacts. To examine the contacts further, for both injection and extraction processes, we performed CTLM measurements over a wide current range. Figure 4c shows the variation of the device parameters with the current level for both current injection and extraction in several different test structures. Achieving the same device parameters for both forward and reverse bias, within the experimental error, for over 4 orders of magnitude variation in current indicates that there is no injection barrier between gold and graphene and that Au/graphene contact is Ohmic. We note that correct evaluation of device parameters using any TLM method requires a graphene layer with a uniform sheet resistance. Contact formation by direct deposition of metal onto graphene induces damage such as unintentional doping that alters the uniformity of the sheet resistance under the contact area. Hence, the uniformity of the sheet resistance is disrupted, and the extracted transfer length, Lt, cannot be correctly interpreted. Using conformal transfer, however, unintentional doping in prevented. Nevertheless the question regarding the validity of the extracted transfer length, Lt, remains open because we have assumed constant sheet resistance for the graphene layer everywhere, for which there is no valid experimental evidence at this point.

To be a viable technology, conformal transfer should produce statistically similar devices. To determine the parameter spread we measured 64 different CTLM test structures. In total more than 600 devices were measured. Values extracted for the sheet resistance, R_{sh}, contact resistance, R_c, and transfer length, L_t, are presented in the histograms of Figure 5. The histograms show a very narrow distribution for each of the device parameters. The fully drawn red curve is a Gaussian distribution fitted to the histograms. Very narrow distributions with good fit qualities, R^2, are achieved. A clear indication that the graphene devices are statistically similar. The mean values achieved for R_{sh}, R_c, and L_t, amount to 500 Ω/□, 980 Ωμm, and 2.02 μm, respectively. The conformal transfer process technology can therefore be used as a platform to fabricate reproducible devices that operate reliably over a broad current range.

We further note that the device parameters did not show significant changes as the temperature was lowered. At low temperatures, down to 30 K, R_c and L_t did not show any systematic change and remained temperature independent. At the same time, R_{sh} showed a steady decrease by only a factor of 2 at 30 K compared to its room temperature value.

FIELD-EFFECT TRANSISTORS

The device parameters of Figures 4 and 5 were extracted using a floating back gate. Because the parameters may depend on the charge carrier density, they were extracted as a function of gate bias. A constant current at different levels was forced between the inner and the surrounding electrode. The voltage drop

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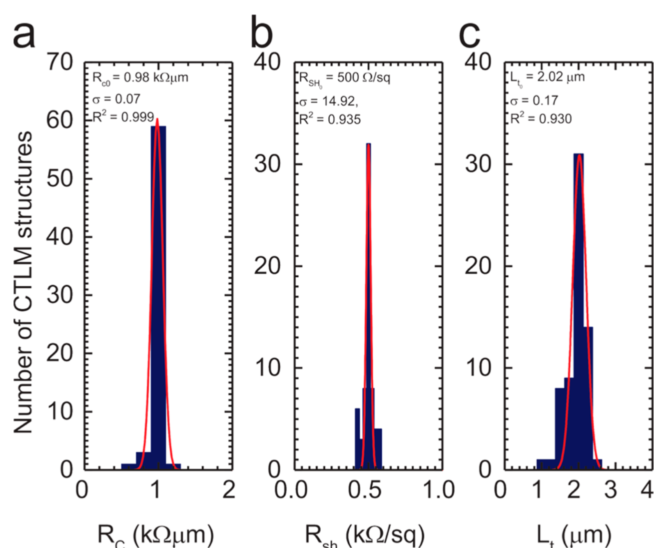

Figure 5. Device parameter spread. Extracted values for the (a) sheet resistance, R_{sh}, (b) contact resistance, R_c, and (c) transfer length, L_t, measured for 64 different CTLM structures. For all measurements, the current level was fixed at 100 μA. The fully drawn curve is a Gaussian fit to the data. The insets present mean values for the R_c, R_{sh}, and L_t extracted from the Gaussian fits, σ is the width of the Gaussian, and R^2 represents the fit quality.

between the source and drain electrodes was measured as a function of gate bias. Figure 6a–c shows the extracted sheet

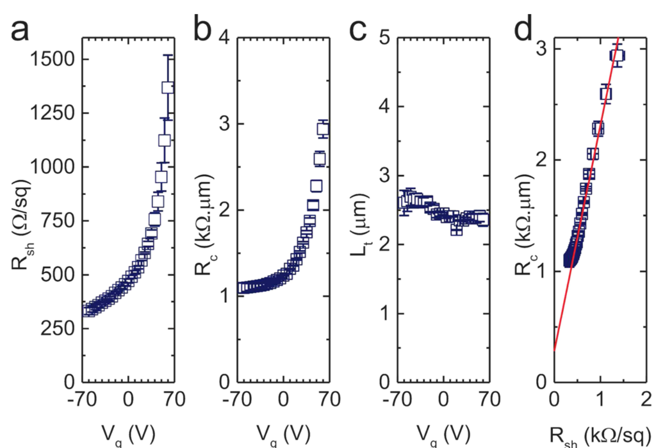

Figure 6. Gate bias dependence. (a,b,c) Values for the sheet resistance, R_{sh}, contact resistance, R_c, and transfer length, L_t, extracted from CTLM measurements as a function of applied gate bias. (d) Contact resistance plotted as a function of sheet resistance on a linear scale.

resistance, the contact resistance, and the transfer length. The sheet resistance, shown in Figure 6a, gradually increases with increasing positive gate bias. The CVD graphene is p-type doped, and with increasing gate bias the graphene channel gets depleted from holes. The charge neutrality, or Dirac, point is beyond 60 V and experimentally not accessible. We note that the shift of the Dirac point to positive gate voltages is typical for CVD graphene.[16] From the gate bias dependence we calculate a hole mobility of 2500 $cm^2/(V\ s)$.

The charge injection takes place on top of the contact, as schematically depicted in Supporting Information Figure S6. Graphene lying on the contact is decoupled from the gate electrode. Hence, when the gate bias varies the change in sheet resistance takes place only in the channel between the source and drain electrode. On top of the metal electrodes, graphene does not experience the gate field, because of screening by the Au electrodes. Consequently, the transfer length, as shown in Figure 6c, does not show any pronounced dependence on the gate bias and remains unchanged for different gate voltages.

The contact resistance depends on the gate bias. The dependence is comparable to that of the sheet resistance. When the contact resistance is plotted as a function of sheet resistance, a linear relation is found, as shown in Figure 6d, which can be used to estimate the lowest attainable contact resistance for Au on CVD graphene. Extrapolation of R_c to zero sheet resistance yields a minimum contact resistance of 280 Ω μm. The value that is only 4–6 times the calculated minimum achievable resistance.[14] We note that theoretical relationships between R_c and R_{sh} for graphene have been predicted.[14,21,22,24] The exact mechanism however is yet to emerge and is beyond the scope of this paper.

The low sheet resistance of the graphene transistors suggests application in analog RF circuits, where the transistor should sustain high current densities. To estimate the maximum achievable current density we measured the output characteristics of the devices at zero gate bias. The $I_{ds} - V_{ds}$ characteristics, presented in Figure 7, are linear up to the highest measured current of 0.5 A. By using the transfer length for graphene transistors extracted from Figure 6, we calculate that the current density supplied by the contact reaches values as high as 10^8 A/m^2. The current density passing through the graphene layer, assuming a thickness of 1 nm, then is in excess of 10^{11} A/m^2, which to the best of our knowledge is the highest reported current density supplied by a transferred CVD graphene device. The mere fact that the source-drain electrodes can reliably supply such a large current density without failure points toward the good quality of the Au–graphene contact formed by conformal transfer.

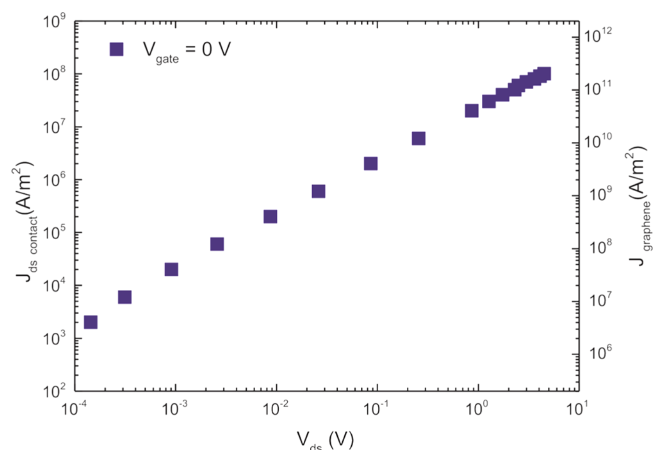

Figure 7. Maximum achievable current density in graphene transistors. A typical output characteristic of a graphene transistor at zero gate bias where current density is given as a function of source-drain bias. A linear dependence is obtained up to the highest current level of 0.5 A. Current density sustained by the electrodes is calculated from the transfer length and the device dimensions. Current density through graphene is calculated with the assumption of a 1 nm layer thickness.

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CONCLUSION

We have presented conformal transfer of CVD graphene as a new technology for reproducible fabrication of graphene devices. The metal−graphene contacts are Ohmic, and show low contact resistances. Conformal transfer is scaled-up to 150 mm wafer technology with a device yield close to unity. The small parameter spread in extracted device parameters shows that the conformal transfer technology yields reproducible devices. The metal−graphene contacts did not experience any further post-fabrication treatments. Even higher contact quality, i.e., lower contact resistance, is anticipated upon conventional contact treatments such as thermal annealing. The immediate impact of conformal transfer technology is that it can be employed as a technique to reliably investigate the fundamental device physics of 2D materials.

METHODS

Graphene films were fabricated using methane as the precursor gas and copper foil (Alfa Aesar, 99.8%) as the metal catalyst in a cold walled CVD reactor (Aixtron).

Electrical measurements were carried out using a cascade M-150 manual probe station, equipped with DCM 210 precision micro-positioners, connected to a Keithley 225 dc current source. For 4-point probe measurement, a constant current was forced. The voltage drop was measured using a Keithley 2400. For gated 4-point probe, the voltage drop as a function of gate bias was measured using a Keithley 4200 SCS with preamplifiers, using triaxial connections. The current was injected or extracted only from the middle electrode. The surrounding electrode was grounded. The voltage difference between these two electrodes was measured by another set of probes. The experiments were carried out at ambient conditions. To inspect the Ohmicity of the contacts, we forced 4 different current levels of ±10 μA, ±100 μA, ±1 mA, and ±10 mA, where + sign refers to charge injection and − refers to charge extraction, respectively. For each current level, the voltage difference was recorded, and the total device resistance was calculated. For temperature dependent experiments, all electrical measurements were conducted in a cryogenic probe station (Janis Research Co.) with a base pressure of 10^{-5} mbar.

ASSOCIATED CONTENT

Supporting Information

Raman spectra and optical images of transferred CVD graphene on the test substrates. A brief description of both TLM and CTLM. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.5b01869.

AUTHOR INFORMATION

Corresponding Author

*E-mail: asadi@mpip-mainz.mpg.de.

Notes

The authors declare no competing financial interest.

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